The CD4068B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline package (NSR suffix), and in chip form (H suffix).

Features:
- Medium-Speed Operation: 
  \[ t_{PH} < t_{PLH} < 75 \text{ ns (typ.) at } V_{DD} = 10 \text{ V} \]
- Buffered inputs and outputs
- 5-V, 10-V, and 15-V parametric ratings
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 \( \mu \text{A} \) at 18 V
- Over full package-temperature range: 100 \( \text{nA} \) at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at \( V_{DD} = 5 \) V
  2 V at \( V_{DD} = 10 \) V
  2.5 V at \( V_{DD} = 15 \) V
- Meets all requirements of JEDEC Tentative Standard No. 138, "Standard Specifications for Description of 'B' Series CMOS Devices"
CD4068B Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, $V_{DD}$
- Voltages referenced to $V_{SS}$ Terminal
  - $-0.5V$ to $+20V$

INPUT VOLTAGE RANGE, ALL INPUTS
- $-0.5V$ to $V_{DD} +0.5V$

DC INPUT CURRENT, ANY ONE INPUT
- $\pm 10mA$

POWER DISSIPATION PER PACKAGE ($P_D$):
- For $T_A = -55^\circ C$ to $+100^\circ C$ ......................................................... 500mW
- For $T_A = +100^\circ C$ to $+125^\circ C$ ......................................................... Derate Linearity at 12mW/$^\circ C$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types) .................. 100mW

OPERATING-TEMPERATURE RANGE ($T_A$)
- $-55^\circ C$ to $+125^\circ C$

STORAGE TEMPERATURE RANGE ($T_{stg}$)
- $-65^\circ C$ to $+150^\circ C$

LEAD TEMPERATURE (DURING SOLDERING):
- At distance $1/16 \pm 1/32$ inch ($1.59 \pm 0.79$mm) from case for 10s max ......................... $+265^\circ C$

Fig. 4 - Typical output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS
CD4068B Types

Fig. 9 - Typical voltage transfer characteristics (NAND output).

Fig. 10 - Typical dynamic power dissipation as a function of frequency.

Fig. 11 - Quiescent-device-current test circuit.

Fig. 12 - Input current test circuit.

Fig. 13 - Input-voltage test circuit.

Fig. 14 - Dynamic power dissipation test circuit.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^-3 inch).
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